

This is a high performance HD compression core IP that implements the VC-1 video coding standard using the advanced profile at level 3.

VC-1 is an informal reference to the SMPTE 421M video codec standard, also commonly called WMV-HD or WVC1. Originally developed by Microsoft, this state-of-the-art compression standard is very comparable to H.264.

Our core is designed to provide high compression levels while preserving image quality; this encoder can compress HD and SD video with high fidelity to minimal bitrate streams.

Superior quality video at low bit rates is achieved by using such features as our high performance motion estimation engine and intelligent frame skip. The latter can reduce an HD image down to only 32-bits without any perceived reduction in image quality.

Supported resolutions range from 64x64 pixels through 2048x2084, including standard resolutions such as QCIF, CIF, D1, 720p, etc...

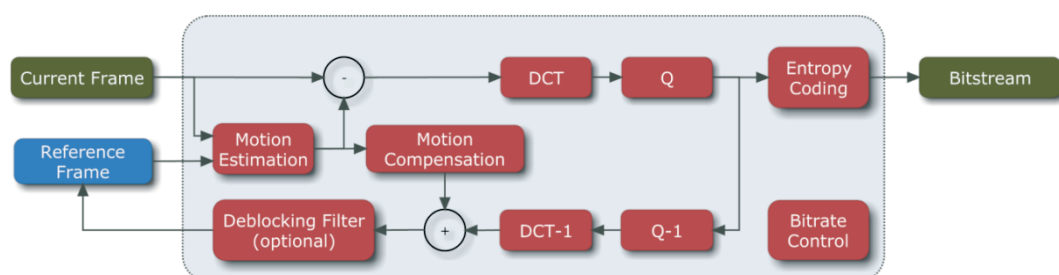
- Only 133MHz required for 1080p at 30fps compression
- Very low latency
- All resolutions and frame rates supported
- Large 1024x512 motion estimation search range
- Bitrates from 64Kbit/s to 80Mbit/s
- SMPTE 421M/ VC-1 Advanced profile @ level 3
- Easily implemented in low cost FPGA

Frame rates are only limited by clock frequency. At 133MHz 1920x1088 pictures can be processed at 30 frames per second.

Our core does not require an external CPU for operation. Optionally, a CPU can be used for encoder configuration or bitstream data transfer.

As the core operates at 133MHz for all HDTV resolutions, it can be easily implemented in a low cost FPGA.

Enciris encoder IP



Key Features

- ❖ Compliant with International Standard specification SMPTE 421M
- ❖ WMV-HD, WVC1 compliant
- ❖ VC-1 Advanced profile @ level 3
- ❖ Very low latency
 - Less than 3ms at 30fps
- ❖ Very efficient processing
 - Only 133MHz for 1920x1088@30fps
- ❖ Motion estimation
 - 1024x512 full pel search range
 - Sub-pixel search
 - Optional output of all Motion Vectors
- ❖ Bitrate control
 - Rate distortion optimization algorithm
 - VBR(variable bitrate) and CBR (constant bitrate) control
 - From 64Kbit/s up to 80Mbit/s
- ❖ Entropy coding
 - Optimized table selection
 - Adaptively insert entry points for error resilience, decoder startup in active streams, and to facilitate editing
 - High throughput
- ❖ Texture coding
 - Precision forward DCT and inverse DCT and quantization
- ❖ Arbitrary resolutions supported
 - All standard resolutions such as QCIF, CIF, D1, 720P, 1080P
 - Any multiple of 16 resolution
- ❖ In-loop filter (option)
- ❖ Fully synchronous design
- ❖ No CPU required for encoding
- ❖ Few internal memory resources
- ❖ 133MHz operation in low cost Lattice ECP2/M FPGA
- ❖ Available for ASIC

Decoder IP: VC1-DEC1

This is a decoder core IP that is fully compatible to the VC1-ENC1 encoder bitstream.

Ideally suited to teleconferencing, video transmission and DVR application, this core can decode HD 1920x1088 at 30 frames per second with only 108MHz clock.

Applications

- ❖ Multimedia systems
- ❖ HDTV
- ❖ Digital video recorders
- ❖ Video Medical systems
- ❖ Video surveillance systems
- ❖ HDTV video cameras

Deliverables

- ❖ EDIF netlist
- ❖ RTL source code
- ❖ Complete testbench
- ❖ Bit accurate C model
- ❖ Complete data sheet

Other IP's

- ❖ Motion estimation Core
- ❖ H.264 CODEC
- ❖ Video preprocessing
- ❖ Multiport DDR memory controller

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