PP-01

Video Preprocessing IP

- Deinterlacing
- Downscaling
- 4:2:2 to 4:2:0 conversion
- Low-Pass filtering
- Arbitrary video resolution
- HDTV applications
- High pixel processing rate
- High performance in low cost FPGA

This all-in-one high performance IP block provides commonly needed video preprocessing functions such as deinterlacing, scaling, and color space downsampling. These functions can be selectively enabled or disabled as required by the system. Designed for high definition video applications, such as HDTV, this IP can process 1-pixel per clock cycle.

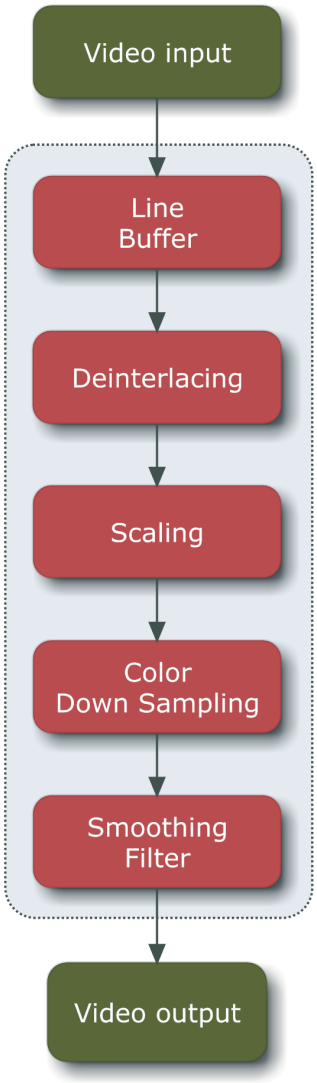
Our advanced deinterlacing filter is designed to process interlaced video sources, such as 480i or 1080i, and output progressive video. A proprietary content/ motion adaptive algorithm reduces to a minimum any combing effects or artifacts commonly associated with other de-interlacing schemes.

Input video can be downscaled by ½ or ¼, using our bicubic scaling function.

Color downsampling is provided by an interpolation algorithm for accurate 4:2:2 to 4:2:0 YCrCb color space conversion, required in high quality HDTV systems.

In addition, a 2-D smoothing system that acts as a low-pass video filter is included. Especially designed for use in video compression applications, the smoothing effect provided can significantly improve peak signal to noise ratio (PSNR) of encoded images, especially in low bitrate applications.

Functional Block Diagram



Key Features

- Accepts 4:2:2 video stream at input
- Outputs 4:2:2 or 4:2:0 video
- Accepts interlaced or progressive video sources
- Four functional blocks
  - Content/motion adaptive deinterlacing that minimizes motion artifacts
    - Can be disabled, if not needed
  - Bicubic downscaling unit
    - No scaling
    - ½ downscaling
    - ¼ downscaling
  - color space conversion
    - 4:2:2 to 4:2:0 downsampling
    - Precision interpolation
    - Disabled for 4:2:2 only applications
  - Smoothing filter
    - Improves peak signal to noise ratio in compression systems
    - Can be disabled
- Arbitrary video resolutions
  - Minimum resolution 16x16
  - Maximum resolution 2048x2048
  - Any horizontal or vertical resolution that is a multiple of 4 is supported.
- Designed to meet HDTV and SDTV requirements
  - 1080i and 1080p
  - 720p
  - 480i and 480p
  - 578i and 576p
- Low latency
  - Only 26 cycles
- High throughput
  - 1 pixel per clock cycle
- Fully synchronous design
- Very high performance in low cost FPGAs
- 180MHz operation for LatticeECP2/M

Applications

- Multimedia systems
- HDTV processing
- Frame grabbers
- Video acquisition
- Video compression systems
- Picture in picture
- Digital video recorders
- Video Medical systems
- Video surveillance systems
- HDTV video cameras
- Industrial video

Deliverables

- EDIF netlist
- RTL source code
- Complete testbench
- Bit accurate C model
- Complete data sheet

Other IP's

- Motion estimation
- Multiport DDR controller
- VC-1 / WMV-HD CODEC
- H.264 CODEC

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