H264-DEC1

H264-HD DECODER IP

A high performance HD compression core IP that implements the H.264 (MPEG-4/AVC) video coding standard using the baseline/main/high profile up to level 5.1.

This decoder core decompresses HD and SD video through the use of advanced algorithms and can be implemented in a low cost FPGA.

Superior quality video at low bit rates is achieved by using such features as our proprietary high performance motion estimation engine, frequency domain noise filtering, and intelligent macroblock skipping (at the encoder side).

Supported resolutions range from 64x64 through 2048x2048 pixels, including all standard resolutions such as QCIF, CIF, D1, 720p, 1080p, 2K, etc. The IP core can also process video at any frame rate. The resulting compressed bit rates can be as low as 64 Kbps or as high as 180 Mbps, depending on content, resolution and frame rate. This wide bit rates range and quality make the core suitable in a very broad range of applications including surveillance, medical, automotive, and broadcasting.

The H.264-DEC1 core has been designed and optimized specifically for use with Lattice Semiconductor ECP3 and ECP2/M FPGAs. A block diagram of the IP decoder core is given below.

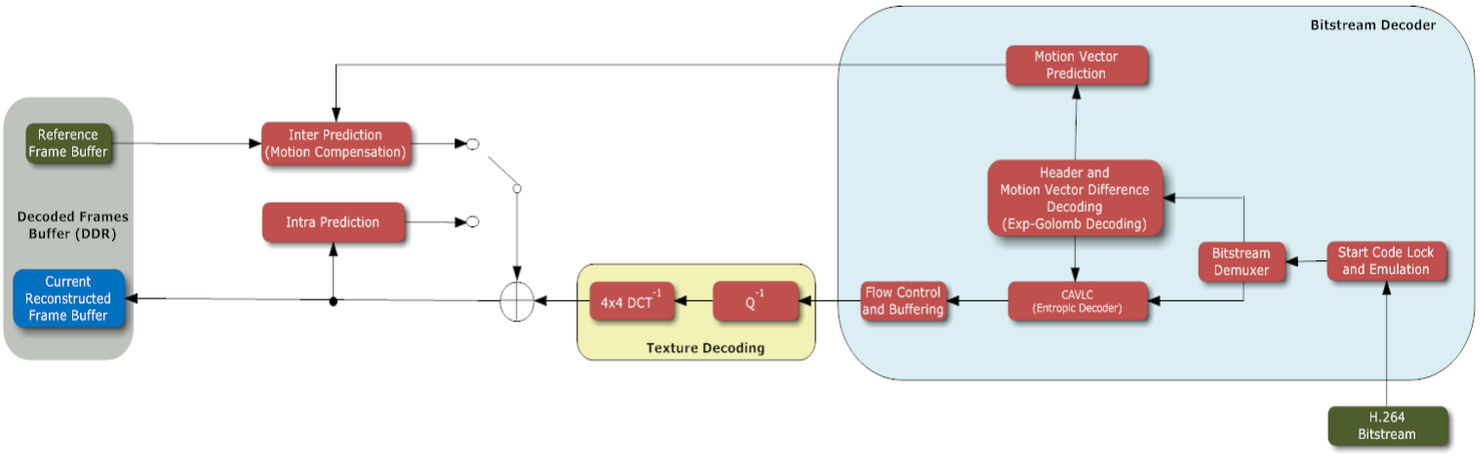
- Only 111.1 MHz required for 1080p at 30 fps compression for the decoding core, and 150.1 MHz for the other processing cores.
- ~11K (I-frame only version) or 12K (I and P frames) LUTs on a Lattice ECP2-70/ECP3-70 FPGA.
- Very low latency.
- All resolutions up to 2048x2048 and frame rates supported.
- Bitrates from 64 Kbps to 180 Mbps.
- H.264 Constrained Baseline, Main and High Profiles up to Level 5.1.
- Several versions available: I-frame only, I/P frames, basic features, and full-features (optimized algorithms).

Frame rates are only limited by clock frequency. At 111.1 MHz 1920x1088 pictures can be processed at 30 frames per second.

Our core does not require an external CPU for operation. Optionally, a CPU can be used for decoder configuration or bitstream data transfer.

As the core operates at 111.1 and 150.1 MHz for all HDTV resolutions, it can be easily implemented in a low cost FPGA.

Enciris Decoder IP



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Key Features

- Compliant with the international ISO/CEI MPEG-4 Part 10 H.264 Standard (ISO/CEI 14496-10)
- H.264 constrained baseline / main / high profile up to level 5.1
- Very low latency
  - Less than 8 ms at 30 fps
- Very efficient processing
  - Only 111.1 MHz for 1920x1088@30fps
- Motion compensation interpolation
  - 32x21 pixels (luma)
  - 32x9 pixels (chroma),
  - 6 and 4-tap filters (luma / chroma)
  - 1/4 and 1/8 pixel resolution (luma/chroma).
- Bitrate control
  - VBR (variable bitrate) and CBR (constant bitrate) control
  - From 64 Kbps up to 180 Mbps
- Entropy coding
  - CAVLC
  - High throughput
- Texture decoding
  - 4x4 precision inverse DCT and inverse quantization
- Arbitrary resolutions supported
  - All standard resolutions such as QCIF, CIF, D1, 720P, 1080p
  - Any multiple of 16 resolution
- Fully synchronous design
- Few internal memory resources
- 111.1 MHz operation for the bitstream decoding core in low cost Lattice ECP2/M and ECP3 FPGAs

Applications

- Multimedia systems
- HDTV
- Digital video recorders
- Medical video systems
- Video surveillance systems
- HDTV video cameras
- Automative video cameras

Deliverables

- EDIF netlist
- Executable binary enabling to generate test-bench files for Verilator simulations
- IP core data sheet
- IP core instantiation manual

Other IPs

- Motion estimation core
- H.264 encoder (EH264ENC1)
- Video preprocessing
- Multiport DDR memory controller

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